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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,168	SCHEFFEL, KLAUS	
	Examiner	Art Unit	
	Jason M. Perilla	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,11-17,21-28,32 and 33* is/are rejected.

7)☒ Claim(s) *8-10,18-20 and 29-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 are pending in the instant application.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on April 20, 2004 and September 23, 2005 are in compliance with the provisions of 37 CFR § 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Europe on January 22, 2004. It is noted, however, that applicant has not filed a certified copy of the application as required by 35 U.S.C. § 119(b). A full copy of the priority document has not been received.

Claim Objections

4. Claim 2 is objected to because of the following informalities:

Regarding claim 2, in line 2, "clocks within the transmitter to the same frequency" should be replaced by –within the transmitter to the same frequency--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 6, 11-14, 16, 21-24, 26, 27, 32, and 33 are rejected under 35 U.S.C. § 102(b) as being anticipated by Benayoun et al (U.S. Pat. No. 5790608; "Benayoun").

Regarding claim 1, Benayoun discloses a method for synchronizing a transmitter and a receiver (abstract), comprising the steps of: generating, by the transmitter (fig. 3A), phase difference information (fig. 3A, "D0-D7") indicating a phase difference between an internal clock (fig. 3A, "CLK2") and an external clock (fig. 3A, "CLK1"); transmitting, by the transmitter, the phase difference information to the receiver (col. 4, lines 50-55); and generating, by the receiver (fig. 3B), a clock signal ("VIDEO CLOCK") dependent on the transmitted phase difference information (fig. 3B, "D0-D15").

Regarding claim 2, Benayoun discloses the limitations of claim 1 as applied above. Further, Benayoun discloses that the internal clock (fig. 6, "CLK1") and the external clock (fig. 6, "CLK2") are frequency-divided (fig. 6, refs. 300 and 310) within the transmitter to the same frequency, the method further comprising the step of converting (fig. 6, ref. 340 and 350) the phase difference between the frequency-divided clocks to a numerical value (fig. 6, "D0-D7") to be transmitted to the receiver.

Regarding claim 3, Benayoun discloses the limitations of claim 2 as applied above. 3. Benayoun further discloses the step of applying pulses of the frequency-divided clocks (fig. 6, refs. 300 and 310) to start and stop inputs of a counter (fig. 6, refs. 340 and 360) which generates the numerical value to be transmitted to the receiver.

Regarding claim 4, Benayoun discloses the limitations of claim 1 as applied above. Further, Benayoun discloses the step of transmitting the phase difference information to the receiver in the form of "SDLC" or multicast packets (col. 4, line 54).

Regarding claim 6, Benayoun discloses the steps of generating, by the receiver (fig. 3B), an internal clock or recovering the internal clock of the transmitter from information received from the transmitter ("NETWORK CLOCK"); frequency-dividing (230), by the receiver, the internal clock; and adjusting (fig. 3B, ref. 231), by the receiver, the phase of the frequency-divided clock based on the received phase difference information (fig. 3B, "D0-D15; col. 5, lines 5-25).

Regarding claim 11, Benayoun discloses a system for synchronizing a transmitter and a receiver (abstract), the system comprises: a transmitter (fig. 3A) comprising a phase difference information generating means (fig. 3A, ref. 281) for generating phase difference information indicating a phase difference between an internal clock (fig. 3A, "CLK2") and an external clock (fig. 3A, "CLK 1"), and transmitting means for transmitting the phase difference information to the receiver (fig. 3A, refs. 260, 190, and 270) ; and a receiver (fig. 3B) comprising a clock generator means (fig. 3B, ref. 231) for generating a clock signal (fig. 3B, "VIDEO CLOCK") dependent on the transmitted phase difference information.

Regarding claim 12, Benayoun discloses the limitations of claim 11 as applied above. Further, Benayoun discloses a frequency divider means (fig. 6, refs. 300 amd 310) for frequency dividing the internal clock and the external clock to the same frequency; and a converting means (fig. 6, refs. 340 and 350) for converting the phase difference between the frequency-divided clocks to a numerical value to be transmitted to the receiver.

Regarding claim 13, Benayoun discloses the limitations of claim 12 as applied above. Further, Benayoun discloses that the converting means (fig. 6) comprises a counter (fig. 6, refs. 340 and 350) which generate the numerical value to be transmitted to the receiver, the counter having start and stop inputs to which pulses of the frequency-divided clocks are applied.

Regarding claim 14, Benayoun discloses the limitations of claim 11 as applied above. Further, Benayoun discloses the step of transmitting the phase difference information to the receiver in the form of "SDLC" or multicast packets (col. 4, line 54).

Regarding claim 16, Benayoun discloses the limitations of claim 11 as applied above. Further, Benayoun discloses that the receiver further comprises: a means (fig. 3B, ref. 190) for generating an internal clock, or for recovering the internal clock of the transmitter (fig. 3B, "NETWORK CLOCK") from information received from the transmitter; a frequency-dividing means (fig. 3B, ref. 230) for frequency-dividing the internal clock; and an adjusting means (fig. 3B, ref. 231) for adjusting the phase of the frequency-divided clock based on the received phase difference information.

Regarding claim 21, Benayoun discloses a transmitter used in a system for synchronizing a transmitter and a receiver (abstract), wherein the receiver comprises a clock generator means (fig. 3B, ref. 231) for generating a clock signal (fig. 3B, "VIDEO CLOCK") dependent on the transmitted phase difference information (fig. 3B, "D0-D15), the transmitter (fig. 3A) comprising: a phase difference generating means (fig. 3A, ref. 281) for generating phase difference information (fig. 3A, "D0-D7) indicating a phase difference between an internal clock (fig. 3A, "CLK1") and an external clock (fig. 3A,

"CLK2"); and a transmitting means (fig. 3A, refs. 260, 190, and 270) for transmitting the phase difference information to a receiver.

Regarding claim 22, Benayoun discloses the limitations of claim 21 as applied above. Further, Benayoun discloses a frequency divider means (fig. 6, refs. 300 amd 310) for frequency dividing the internal clock and the external clock to the same frequency; and a converting means (fig. 6, refs. 340 and 350) for converting the phase difference between the frequency-divided clocks to a numerical value to be transmitted to the receiver.

Regarding claim 23, Benayoun discloses the limitations of claim 22 as applied above. Further, Benayoun discloses that the converting means (fig. 6) comprises a counter (fig. 6, refs. 340 and 350) which generate the numerical value to be transmitted to the receiver, the counter having start and stop inputs to which pulses of the frequency-divided clocks are applied.

Regarding claim 24, Benayoun discloses the limitations of claim 21 as applied above. Further, Benayoun discloses the step of transmitting the phase difference information to the receiver in the form of "SDLC" or multicast packets (col. 4, line 54).

Regarding claim 26, Benayoun discloses a receiver (fig. 3B) , used in a system for synchronizing a transmitter and a receiver (abstract), wherein the transmitter (fig. 3A) comprises a phase difference generating means (fig. 3A, ref. 281) for generating phase difference information (fig. 3A, "D0-D7") indicating a phase difference between an internal clock (fig. 3A, "CLK2") and an external clock (fig. 3A, ref. "CLK1") and means for transmitting (fig. 3A, refs. 260, 190, and 270) the phase difference information to the

receiver, the receiver comprising: a clock generator means (fig. 3B, ref. 231) for generating a clock signal dependent on a phase difference information (fig. 3B, ref. "D0-D15") transmitted from a transmitter.

Regarding claim 27, Benayoun discloses the limitations of claim 26 as applied above. Benayoun further discloses means (fig. 3B, ref. 190) for generating an internal clock (fig. 3B, "NETWORK CLOCK"), or for recovering the internal clock of the transmitter from information received from the transmitter; a frequency-dividing means (fig. 3B, ref. 230) for frequency-dividing the internal clock; and an adjusting means (fig. 3B, ref. 231) for adjusting the phase of the frequency-divided clock based on the received phase difference information (fig. 3B, "D0-D15").

Regarding claim 32, Benayoun discloses a method for synchronizing a transmitter and a receiver (abstract) wherein the receiver (fig. 3B) generates a clock signal (fig. 3B, "VIDEO CLOCK") dependent on a transmitted phase difference information (fig. 3B, "D0-D15"), the method comprising the steps of: generating, by a transmitter (fig. 3A), phase difference information (fig. 3A, "D0-D7") indicating a phase difference between an internal clock (fig. 3A, "CLK1") and an external clock (fig. 3A, "CLK2"); and transmitting (fig. 3A, refs. 260, 190, and 270), by the transmitter, the phase difference information to the receiver.

Regarding claim 33, Benayoun 33 a method for synchronizing a transmitter and a receiver (abstract) wherein the transmitter (fig. 3A) generates phase difference information (fig. 3A, "D0-D7) indicating a phase difference between an internal clock (fig. 3A, "CLK1") and an external clock (fig. 3A, "CLK2") , the method comprising the

step of: generating, by the receiver, a clock signal (fig. 3B, "VIDEO CLOCK") dependent on a transmitted phase difference information (fig. 3B, "D0-D15") indicating a phase difference between the internal and the external clock of the transmitter, the phase difference information being received from the transmitter.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5, 15, and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Benayoun.

Regarding claim 5, Benayoun discloses the limitations of claim 1 as applied above. Benayoun does not explicitly disclose the frequencies of the internal or external clocks (i.e. fig. 3A, "CLK1" and "CLK2") and does not disclose that the internal clock has a frequency of 80 MHz or 89.6 MHz and the external clock has a frequency of 2.048 MHz or 1.544 MHz. However, the specification of the instant invention does not provide any particular reason for the use of such frequencies and does not provide any indication of non-obviousness associated with such frequencies. Furthermore, one skilled in the art would find that any frequencies could be utilized because the invention is based upon determining a difference in phase which could be applied between any two frequencies. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to use frequencies of 80 MHz, 89.6

MHz, 2.048 MHz, or 1.544 MHz as the internal and external clock frequencies because, as understood by one having ordinary skill in the art, the frequency analyzed is arbitrary and could be tailored depending upon the design considerations.

Regarding claim 15, Benayoun discloses the limitations of claim 11 as applied above. Further, the remaining limitations of the claim are obvious as applied to in claim 5 above.

Regarding claim 25, Benayoun discloses the limitations of claim 21 as applied above. Further, the remaining limitations of the claim are obvious as applied to in claim 5 above.

9. Claims 7, 17 and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Benayoun in view of Knapp et al (U.S. Pat. No. 7106224; "Knapp").

Regarding claim 7, Benayoun discloses the limitations of claim 6 as applied above. Benayoun does not explicitly disclose the step of multiplying, by the receiver, the frequency of the adjusted frequency-divided clock for generating an external clock. Rather, Benayoun discloses applying the adjusted frequency-divided clock (fig. 3B, output of ref. 230) to a VCO (fig. 3B, ref. 231) for phase adjustment according to the phase offset received (fig. 3B, ref. "D0-D15). It is implied that the "VIDEO CLOCK" of Benayoun is of a higher frequency than the received "NETWORK CLOCK" but it is not explicitly disclosed. However, Knapp teaches that network clock signals are typically multiplied to achieve desired local frequencies (fig. 8, ref. 74; col. 13, lines 55-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time

which the invention was made that the "NETWORK CLOCK" of Benayoun could be multiplied, at least in part, to determine the desired local "VIDEO CLOCK" as taught by Knapp because the determination of a local clock by multiplication is well known in the art as being an effective and simple method to achieve the generation of a particular frequency.

Regarding claim 17, Benayoun discloses the limitations of claim 16 as applied above. Further, Knapp discloses the remaining limitations of the claim as applied in claim 7 above.

Regarding claim 28, Benayoun discloses the limitations of claim 26 as applied above. Further, Knapp discloses the remaining limitations of the claim as applied in claim 7 above.

Allowable Subject Matter

10. Claims 8-10, 18-20, and 29-31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art of record not relied upon above is cited to further show the state of the art with respect to phase synchronization.

U.S. Pat. No. 7116686 to Van Der Putten et al.

U.S. Pat. No. 6917656 to Fuhrmann et al.

U.S. Pat. No. 6275549 to Greatwood et al.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jason M. Perilla
June 25, 2007

jmp

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER